	Application No.	Applicant(s)
Notice of Allowability	09/458,121	MOAS ET AL.
	Examiner	Art Unit
	Tuan A. Vu	2193

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/13/06*.

2. ☒ The allowed claim(s) is/are *1-2, 4, 6-11, 13, 15-18 (renum 1-14)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some*   c) ☐ None of the:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the

         International Bureau (PCT Rule 17.2(a)).

    * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

    (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached

        1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____ .

    (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of

        Paper No./Mail Date *12/07/06*.

    Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)

2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)

3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____

4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

5. ☐ Notice of Informal Patent Application

6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *12/06/06* .

7. ☒ Examiner's Amendment/Comment

8. ☒ Examiner's Statement of Reasons for Allowance

9. ☐ Other _____ .

DETAILED ACTION

1.   This action is responsive to the Applicant's response filed 11/13/06.

As indicated in Applicant's response, claims 1-2, 4-11, 13-18 have been amended, and

claims 22-25 canceled. Claims 1-2, 4-11, 13-18 are pending in the office action.

EXAMINER'S AMENDMENT

1.   An examiner's amendment to the record appears below. Should the changes and/or

additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR

1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the

payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with

Mark Watson, Reg # 46,322 on 12/06/06.

The application has been amended as follows:

In the CLAIMS:

Claim 1:

A method comprising:

inserting a single instruction at the block header of a block of code configured for

execution on a first processor architecture, wherein the single instruction is to determine if

~~processor~~ resources needed <u>for the first processor</u> to execute the block of code are available;

emulating the block of code on ~~a computer system configured for execution on~~ a second

processor <u>corresponding to a second</u> architecture;

using the single instruction to monitor the resources of the ~~computer system~~ <u>second</u>

<u>processor</u> used during emulation <u>at the second processor</u> to determine whether resource

requirements of the first processor architecture have been exceeded, <u>wherein the single</u>

<u>instruction dynamically generates one or more bit vectors to represent the resources of the</u>

<u>second processor architecture</u>;

    if the resource requirements of the first processor architecture have been exceeded,

modifying allocation of the resources of the ~~computer system~~ <u>second processor</u> according to the

resource requirements of the first processor architecture; and

    if the resource requirements of the first processor architecture have been not exceeded,

continuing emulation of the block of code.

Claim 4:

    The of claim 1 wherein the availability of the resources of the ~~computer system~~ <u>second</u>

<u>processor</u> is determined at compile time.

Claim 5:   (Cancelled)

Claim 6:

    The method of claim 1 further comprising:

    signaling an error message if the resources of the ~~computer system~~ <u>second processor</u>

needed to execute the block of code are not available; and

    in response to the error message, branching to a fault handler routine.

Claim 8:

    The method of claim 1 ~~wherein the resources of the computer system are represented by a~~

<u>wherein dynamically generating the</u> bit vector<u> comprises generating intermediate arrays</u>.

Claim 9:

The method of claim 8 wherein the ~~bit vector is generated dynamically~~ <u>intermediate</u> <u>arrays comprise a first array to represent an expected status and a second array to represent a</u> <u>current status</u>.

Claim 10:

A computer-readable medium having stored thereon a set of instructions to monitor processor resources, said set of instruction, which when executed by a processor, cause said processor to perform a method comprising:

inserting a single instruction at the block header of a block of code configured for execution on a first processor architecture, wherein the single instruction is to determine if ~~processor~~ resources needed <u>for the first processor</u> to execute the block of code are available;

emulating the block of code on ~~a computer system configured for execution on~~ a second processor <u>corresponding to a second</u> architecture;

using the single instruction to monitor the resources of the ~~computer system~~ <u>second</u> <u>processor</u> used during emulation <u>at the second processor</u> to determine whether resource requirements of the first processor architecture have been exceeded, <u>wherein the single</u> <u>instruction dynamically generates one or more bit vectors to represent the resources of the</u> <u>second processor</u>;

if the resource requirements of the first processor architecture have been exceeded, modifying allocation of the resources of the ~~computer system~~ <u>second processor</u> according to the resource requirements of the first processor architecture; and

if the resource requirements of the first processor architecture have been not exceeded, continuing emulation of the block of code.

Claim 13:

The computer-readable medium of claim 10 wherein the availability of the resources of

the ~~computer system~~ second processor is determined at compile time.

Claim 14:   (Cancelled)

Claim 15:

The computer-readable medium of claim 10 wherein additional instructions, which when

executed by the processor, cause the processor to perform the method further comprising:

signaling an error message if the resources of the ~~computer system~~ second processor

needed to execute the block of code are not available; and

in response to the error message, branching to a fault handler routine.

Claim 17:

The computer-readable medium of claim 10 ~~wherein the resources of the computer~~

~~system are represented by a~~ wherein dynamically generating the bit vector comprises generating

intermediate arrays.

Claim 18:

The computer-readable medium of claim 17 wherein the ~~bit vector is generated~~

~~dynamically~~ intermediate arrays comprise a first array to represent an expected status and a

second array to represent a current status.

EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

2.   Claims 1-2, 4, 6-11, 13, 15-18 are allowed.

The following is an examiner's statement of reasons for allowance:

The prior art taken separately or jointly does not suggest or teach the following features.

A method for monitoring processor resources comprising (i) inserting a single instruction at the beginning of a block of code configured to be run on a first processor architecture; emulating said block of code on a second processor corresponding to a second architecture, using the single instruction during emulation at the second processor, (ii) the single instruction dynamically generating a bit vector to represent the resources at the second processor; and (iii) to determine thereby whether resource requirements of the first processor architecture have been exceeded such that if said resource requirements have been exceeded, modifying the resources at the second processor according to the requirements of the first processor architecture; and if not continuing emulating the block of code; as recited in claim 1 and 10.

Long, USPN: 5,835,958, discloses invoking a stack resources checking function of a compiled code via trampoline implementation to determine if stack resources would be such as to require allocation of more memory resources to execute the compiled function; but does not suggest nor teach implementation of 2 processors as in (i) to implement emulation of a block of code having an single instruction inserted at the beginning of the block, the block of code configured for the a first processor architecture, the emulation being executed on a second processor of another architecture such that this instruction while executed by the second processor dynamically generates a bit vector as in (ii) to represent the second processor resources, whereby the single instruction can monitor the second processor resources so to determine as in (iii) whether the resources requirements of the first processor have been

exceeded and thus modify the resources of the executing environment of the second processor

according to such requirements.

Yates, USPN: 6,091,897, discloses providing a native environment to execute a non-

native instruction set loaded as a image using an optimizing interpreter; using profiling statistics

during executing at the native platform to observe behavior of the non-native code, e.g. validity

of data within register/stack for a given non-native reference – via analyzing the dependencies of

data among the basic blocks of code running in such native environment; and accordingly

provide adjustment and optimization for the non-native instructions, wherein each block of code

includes an associated internal state container structure represented via a bit vector to

dynamically support the above block dependencies collection. Even though Yates teaches

emulating one set of instruction image in one processor to support optimization of another

processor architecture code; and a bit vector, Yates teaches an extensive implementation of

profile data analysis and accordingly, includes in each non-native block of code a state container

as part of the block to support the data dependencies or displacement verification, thereby

enabling optimized translation of non-native code. Yates, hence does not teach or suggest

creation of a single instruction inserted at the beginning of each such emulated blocks of code to

dynamically create a bit vector representing the resources of each such block at the native

environment and use the bit vector to determine resources threshold-reaching event related to the

resource requirements of the non-native architecture as in (ii) by means of this dynamic bit

vector, modifying the resources of block of code of the native environment emulation process to

meet the above requirements as in (iii).

Any comments considered necessary by applicant must be submitted no later than the

payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for

Allowance."

Drawings

3.   New corrected drawings in compliance with 37 CFR 1.121(d) are required in this

application because according to the response filed 11/10/03 where Fig. 1A-D were to be fixed,

there was mention that attached and corrected copies of drawings were submitted with the

response. Apparently, there has been no evidence of record in regard to any of these drawing

sheets. It is also noted that Drawings Figures 2-3 are still in a hand-written non-official format,

which requires a more legible corresponding copies. A full set of corrected drawings is required

for the record to set clear on this issue.

Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent

and Trademark Office no longer prepares new drawings.

The corrected drawings are required in reply to the Office action prior to payment of the

Issue Fees, to obviate complication to the state of prosecution of the case. The requirement for

corrected drawings will not be held in abeyance as per the current Office Action.

Conclusion

4.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tuan A Vu whose telephone number is (272) 272-3735. The

examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Meng-Ai An can be reached on (571)272-3756.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3735 (for non-official correspondence - please consult Examiner before using) or 571-273-8300 (for official correspondence) or redirected to customer service at 571-272-3609.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan A Vu
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